	Type	L #	Hits	S arch T xt	DBs	Time Stamp
1	BRS	L119	60885	TFT or "thin film transistor"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52
2	BRS	L120	1956099	substrate or wafer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52
3	BRS	L121	1726	(polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52
4	BRS	L125	727	upilex-s or upilex-vt or upilex-50ss or "UBE America"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52
5	IS&R	L127	994	(438/149).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52

	Typ	L #	Hits	S arch T xt	DBs	Tim Stamp
6	IS&R	L129	304	(438/155).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52
7	BRS	L131	315	(substrate base wafer bulk) with (polyphenylene near3 polyimide$2)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:52
8	BRS	L133	875	(substrate base wafer bulk) with (polyphenylene and polyimide$2)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53
9	BRS	L122	2	((substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))) and (TFT or "thin film transistor")	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53
10	BRS	L123	28	(substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53

	Typ	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L124	18	((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)) and (TFT or "thin film transistor")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53
12	BRS	L126	9	(upilex-s or upilex-vt or upilex-50ss or "UBE America") and (TFT or "thin film transistor")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53
13	BRS	L128	2	((438/149).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53
14	BRS	L130	1	((438/155).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53
15	BRS	L132	223	((substrate base wafer bulk) with (polyphenylene near3 polyimide$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 19:53

	Type	L #	Hits	Search T xt	DBs	Tim Stamp
16	BRS	L134	597	((substrate base wafer bulk) with (polyphenylene and polyimide$2)) and (@ad<20000418 @rlad<20000418)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
17	BRS	L135	152	(((substrate base wafer bulk) with (polyphenylene and polyimide$2)) and (@ad<20000418 @rlad<20000418)) and (chip semiconductor)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53

	Typ	L #	Hits	Search T xt	DBs	Tim Stamp
1	BRS	L1	60885	TFT or "thin film transistor"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:44
2	BRS	L2	1956099	substrate or wafer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:45
3	BRS	L4	1726	(polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:45
4	BRS	L6	2	5 and 1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:46
5	BRS	L5	28	2 near4 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:49

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L7	18	4 and 1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:55
7	BRS	L8	727	upilex-s or upilex-vt or upilex-50ss or "UBE America"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 10:55
8	BRS	L9	9	8 and 1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 11:00
9	IS&R	L10	994	(438/149).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 11:00
10	BRS	L11	2	10 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 11:03

	Type	L #	Hits	S arch Text	DBs	Time Stamp
11	IS&R	L12	304	(438/155).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 11:03
12	BRS	L15	1	12 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/11 11:04

	Type	L #	Hits	Search T xt	DBs	Time Stamp
1	BRS	L1	60969	TFT or "thin film transistor"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57
2	BRS	L2	1957373	substrate or wafer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57
3	BRS	L3	1730	(polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57
4	BRS	L4	730	upilex-s or upilex-vt or upilex-50ss or "UBE America"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57
5	IS&R	L5	996	(438/149).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57

	Type	L #	Hits	Search T xt	DBs	Time Stamp
6	BRS	L6	316	(substrate base wafer bulk) with (polyphenylene near3 polyimide$2)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57
7	BRS	L7	877	(substrate base wafer bulk) with (polyphenylene and polyimide$2)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:57
8	IS&R	L17	304	(438/155).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
9	BRS	L8	2	((substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))) and (TFT or "thin film transistor")	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
10	BRS	L9	28	(substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L10	18	((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)) and (TFT or "thin film transistor")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
12	BRS	L11	9	(upilex-s or upilex-vt or upilex-50ss or "UBE America") and (TFT or "thin film transistor")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
13	BRS	L12	2	((438/149).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
14	BRS	L13	223	((substrate base wafer bulk) with (polyphenylene near3 polyimide$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
15	BRS	L14	1	((438/155).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58

	Type	L #	Hits	S arch Text	DBs	Tim Stamp
16	BRS	L15	597	((substrate base wafer bulk) with (polyphenylene and polyimide$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
17	BRS	L16	152	(((substrate base wafer bulk) with (polyphenylene and polyimide$2)) and (@ad<20000418 @rlad<20000418)) and (chip semiconductor)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 12:58
18	IS&R	L18	651	(438/30).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 13:28
19	IS&R	L21	263	(438/152).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/13 14:02

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1 **Application of engineering plastic materials to office automation an audio-visual appliances in Japan**
Yasufuku, S.;
Electrical Insulation Magazine, IEEE , Volume: 8 , Issue: 6 , Nov.-Dec. 1992
Pages:5 - 12

[Abstract] [PDF Full-Text (720 KB)] **IEEE JNL**

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2 **Qualification testing of engineering thermoplastics for electrical distribution applications**
Ferrito, S.J.;
Electrical Insulation and Dielectric Phenomena, 2002 Annual Report Conferen on , 20-24 Oct. 2002
Pages:68 - 71

[Abstract] [PDF Full-Text (386 KB)] **IEEE CNF**

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Thin-film transistors on plastic and glass substrates silicon deposited by microwave plasma ECR-CVD

Lihong Teng Anderson, W.A.
Dept. of Electr. Eng., State Univ. of New York, Buffalo, NY, USA

This paper appears in: **Electron Device Letters, IEEE**

Publication Date: June 2003
On page(s): 399 - 401
Volume: 24 , Issue: 6
ISSN: 0741-3106
Inspec Accession Number: 7701417

Abstract:
Thin-film **transistors** (TFTs) were fabricated on **polyimide** and glass substra temperatures using microwave ECR-CVD deposited amorphous and nanocryst as active layers. The amorphous Si TFT fabricated at 200 /spl deg/C on the p foil had a saturation region field effect mobility of 4.5 cm/sup 2//V-s, a linear mobility of 5.1 cm/sup 2//V-s, a threshold voltage of 3.7 V, a subthreshold sv V/decade, and an ON/OFF current ratio of 7.9 /spl times/ 10/sup 6/. This larg and high ON/OFF current ratio were attributed to the high-quality channel ma less dangling bond defect states. Nanocrystalline Si TFTs fabricated on glass s at 400 /spl deg/C showed a saturation region mobility of 14.1 cm/sup 2//V-s, region mobility of 15.3 cm/sup 2//V-s, a threshold voltage of 3.6 V, and an O current ratio of 6.7 /spl times/ 10/sup 6/. TFT performance was mostly indep substrate type when fabrication conditions were the same.

Index Terms:
amorphous semiconductors carrier mobility dangling bonds elemental semiconducto hydrogen nanostructured materials plasma CVD silicon thin film transistors 200 (V 400 C ON/OFF current ratio Si:H-SiO/sub 2/ TFTs amorphous Si TFT amorph dangling bond defect states glass substrates high-quality channel materials hydroge linear region mobility low temperature fabrication microwave plasma ECR-CVD nano TFTs nanocrystalline silicon polyimide foil polyimide substrates saturation region mobility silicon deposition subthreshold swing thin-film transistors threshold voltag

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1 **DC and microwave noise transient behavior of InP/InGaAs double heterojunction bipolar transistor (DHBT) with polyimide passivation**
Yong Zhong Xiong; Geok-Ing Ng; Hong Wang; Fu, J.S.;
Electron Devices, IEEE Transactions on , Volume: 48 , Issue: 10 , Oct. 2001
Pages:2192 - 2197

[Abstract] [PDF Full-Text (144 KB)] **IEEE JNL**

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2 **Current transient in polyimide-passivated InP/InGaAs heterojuncti bipolar transistors: systematic experiments and physical model**
Hong Wang; Geok-Ing Ng;
Electron Devices, IEEE Transactions on , Volume: 47 , Issue: 12 , Dec. 2000
Pages:2261 - 2269

[Abstract] [PDF Full-Text (172 KB)] **IEEE JNL**

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3 **Polyimide Passivated AlGaN–GaN HFETs With 7.65 W/mm at 18 GH**
Hampson, M.D.; Shen, S.-C.; Schwindt, R.S.; Price, R.K.; Chowdhury, U.; Wo M.M.; Zhu, T.G.; Yoo, D.; Dupuis, R.D.; Feng, M.;
Electron Device Letters, IEEE , Volume: 25 , Issue: 5 , May 2004
Pages:238 - 240

[Abstract] [PDF Full-Text (120 KB)] **IEEE JNL**

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4 **Electron irradiation effects in polyimide passivated InP/InGaAs sin heterojunction bipolar transistors**
Shatalov, A.; Subramanian, S.; Chandrasekhar, S.; Dentai, A.; Goodnick, S.M
Nuclear Science, IEEE Transactions on , Volume: 46 , Issue: 6 , Dec. 1999
Pages:1708 - 1715

[Abstract] [PDF Full-Text (524 KB)] IEEE JNL

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5 **Amorphous silicon thin-film transistors on compliant polyimide foil substrates**
Gleskova, H.; Wagner, S.;
Electron Device Letters, IEEE , Volume: 20 , Issue: 9 , Sept. 1999
Pages:473 - 475

[Abstract] [PDF Full-Text (88 KB)] IEEE JNL

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6 **Base current transient behavior in polyimide-passivated InP/InGaA heterojunction bipolar transistors**
Hong Wang; Geok Ing Ng; McAlister, S.P.;
Indium Phosphide and Related Materials, 2000. Conference Proceedings. 200(International Conference on , 14-18 May 2000
Pages:193 - 196

[Abstract] [PDF Full-Text (260 KB)] IEEE CNF

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7 **Field-induced instabilities in polyimide passivated lateral PNP trans**
El-Kareh, B.; Hook, T.B.; Johnson, M.E.; Lajza, J.J.; McLaughlin, R.W.;
Electronic Components and Technology Conference, 1990. Proceedings., 40th 23 May 1990
Pages:686 - 692 vol.1

[Abstract] [PDF Full-Text (440 KB)] IEEE CNF

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8 **Thin-film transistors on plastic and glass substrates using silicon deposited by microwave plasma ECR-CVD**
Lihong Teng; Anderson, W.A.;
Electron Device Letters, IEEE , Volume: 24 , Issue: 6 , June 2003
Pages:399 - 401

[Abstract] [PDF Full-Text (258 KB)] IEEE JNL

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9 **Field-induced instabilities in polyimide passivated lateral pnp transi**
El-Kareh, B.; Hook, T.B.; Johnson, M.E.; Lajza, J.J.; McLaughlin, R.W.;
Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [also IEEE Trans. on Components, Packaging, and Manufacturing Technology, A, B, C] , Volume: 13 , Issue: 4 , Dec. 1990
Pages:623 - 628

[Abstract] [PDF Full-Text (456 KB)] IEEE JNL

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10 **Reduction of base-collector capacitance in InP/InGaAs HBT's using novel double polyimide planarization process**
Hyunchol Shin; Gaessler, C.; Leier, H.;
Electron Device Letters, IEEE , Volume: 19 , Issue: 8 , Aug. 1998
Pages:297 - 299

[Abstract] [PDF Full-Text (120 KB)] IEEE JNL

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11 **A multilink active catheter with polyimide-based integrated CMOS**

interface circuits
Ki-Tae Park; Esashi, M.;
Microelectromechanical Systems, Journal of , Volume: 8 , Issue: 4 , Dec. 199
Pages:349 - 357

[Abstract] [PDF Full-Text (640 KB)] **IEEE JNL**

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12 **AlGaAs/GaAs HBTs fabricated by a self-alignment technology using polyimide for electrode separation**
Morizuka, K.; Asaka, M.; Iizuka, N.; Tsuda, K.; Obara, M.;
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Pages:598 - 600

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13 **Tri-layer a-Si:H TFTs on polymeric substrates**
Thomasson, D.B.; Bonse, M.; Koval, R.J.; Huang, J.R.; Wronski, C.R.; Jackso T.N.;
Device Research Conference Digest, 1998. 56th Annual , 22-24 June 1998
Pages:126 - 127

[Abstract] [PDF Full-Text (292 KB)] **IEEE CNF**

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14 **Heterojunction bipolar transistors using GaInAs/InP**
Topham, P.J.; Griffith, I.; Riffat, J.; Goodfellow, R.C.;
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Pages:16/1 - 16/4

[Abstract] [PDF Full-Text (104 KB)] **IEE CNF**

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15 **Current analysis of polyimide passivated InGaP/GaAs HBT**
Masum, J.; Parmiter, P.; Hall, T.J.; Crouch, M.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 143 , Issue: 5 , Oct. 1996
Pages:307 - 312

[Abstract] [PDF Full-Text (508 KB)] **IEE JNL**

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16 **Measurement and modeling of high-speed interconnect-limited dig ring oscillators: The effect of dielectric anisotropy**
Garg, A.; Le Coz, Y.L.; Greub, H.J.; McDonald, J.F.; Iverson, R.B.;
Interconnect Technology Conference, 1998. Proceedings of the IEEE 1998 International , 1-3 June 1998
Pages:241 - 243

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

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17 **New method for observation of polyimide adhesion on non-planar surfaces**
Sidorov, V.; Paz, Y.; Ritter, D.;
Adhesive Joining and Coating Technology in Electronics Manufacturing, 1998. Proceedings of 3rd International Conference on , 28-30 Sept. 1998
Pages:202 - 205

[Abstract] [PDF Full-Text (592 KB)] **IEEE CNF**

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18 **DC-gate-bias stressing of a-Si:H TFTs fabricated at 150°C on polyir foil**
Gleskova, H.; Wagner, S.;
Electron Devices, IEEE Transactions on , Volume: 48 , Issue: 8 , Aug. 2001
Pages:1667 - 1671

[Abstract] [PDF Full-Text (124 KB)] **IEEE JNL**

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19 **Micr wave transf rmers, induct rs and transmissi n lines implem in an Si/SiGe HBT process**
Laney, D.C.; Larson, L.E.; Chan, P.; Malinowski, J.; Harame, D.; Subbanna, S Volant, R.; Case, M.;

Microwave Theory and Techniques, IEEE Transactions on , Volume: 49 , Issue 8 , Aug. 2001
Pages:1507 - 1510

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20 **Electron irradiation effects in AlGaAs/GaAs single heterojunction bipolar transistors**
Sarkar, A.; Subramanian, S.; Goodnick, S.M.;
Electron Devices, IEEE Transactions on , Volume: 47 , Issue: 11 , Nov. 2000
Pages:2024 - 2030

[Abstract] [PDF Full-Text (156 KB)] IEEE JNL

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21 **Integration of polyimide waveguides with traveling-wave phototransistors**
Prakash, D.P.; Scott, D.C.; Fetterman, H.R.; Matloubian, M.; Du, Q.; Wang, V
Photonics Technology Letters, IEEE , Volume: 9 , Issue: 6 , June 1997
Pages:800 - 802

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